fiXtress™

BQR
Reliable Engineering
Optimized Maintenance

Dramatically Improve Your Electronic Design Process

Design for Reliability

fiXtress™ - Next Generation (Ver 9.0)

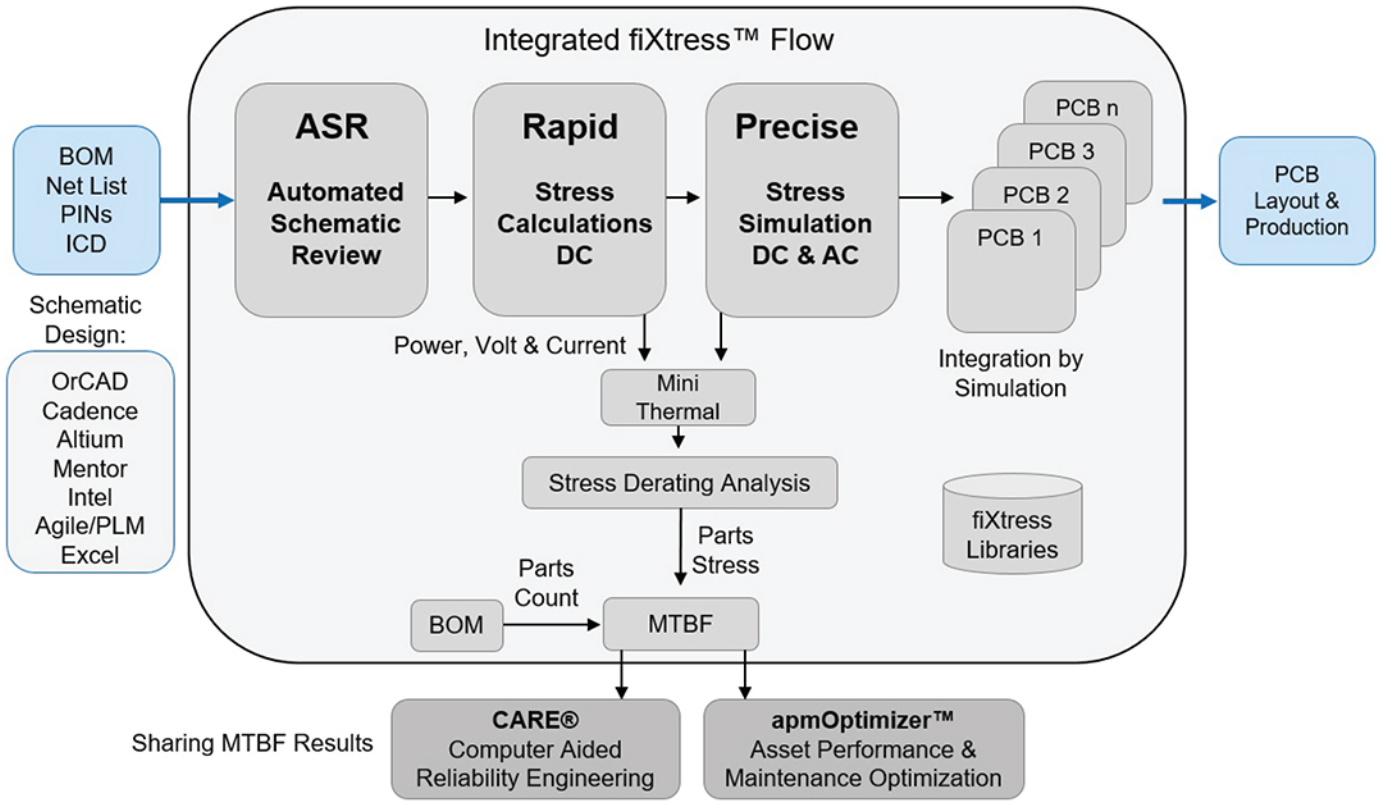
Today's electronic designs are becoming increasingly complex, making it harder to detect errors that generate high costs and hundreds of work hours. Detecting these errors in advance can be instrumental in preventing damages. Unfortunately, in many cases, errors are discovered only in the testing phase or at the customer's site.

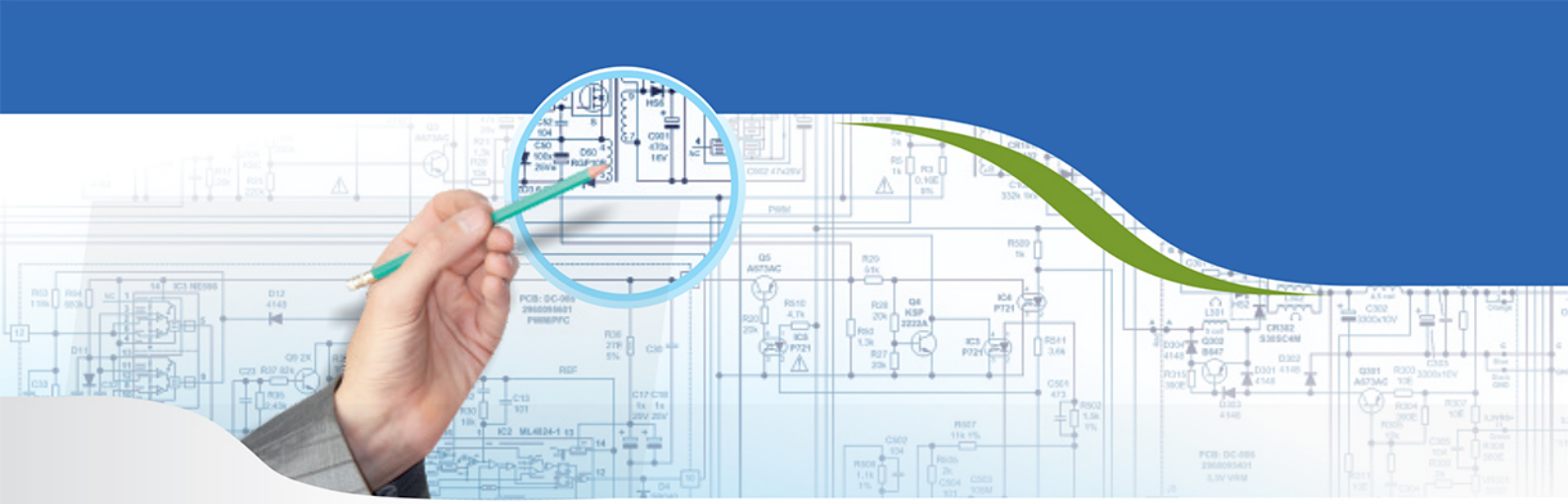
BQR fiXtress is a powerful and unique design error detection and stress analysis tool for electrical circuits. FiXtress detects design errors during the design phase, before layout and production. This way, no schematic, connectivity or stress errors are found in the qualification tests during final verification. fiXtress shortens design cycles and time to market, which saves immense sums as well as bolstering corporate reputation.

fiXtress is a superior Design for Reliability (DfR) suite, serving as an add-on for any Electronic Design Automation (EDA) tool. It is the only tool integrating design error detection with electrical stress, thermal, MTBF and service life prediction at the schematic level, before PCB layout and production. fiXtress modules can either operate standalone, or complement other modules to provide a comprehensive DfR solution for electrical circuits and PCB design.

fiXtress Modules

- ASR - Automated Schematic Review
- Rapid - Electrical Stress Calculation
- Precise - Electrical Stress Simulation
- SDA - Stress Derating Analysis
- MTBF - MTBF Prediction
- Mini Thermal - Calculates dT from environment to PCB
- Multi-Boards Integration - System Level verification
- CAD/CAE Interface - Automatic library preparation



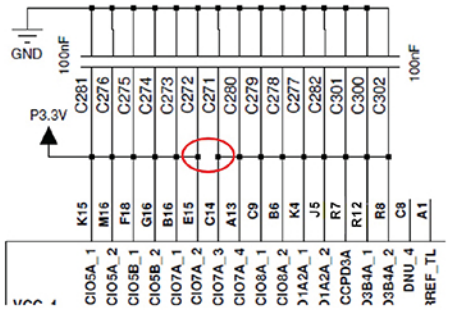


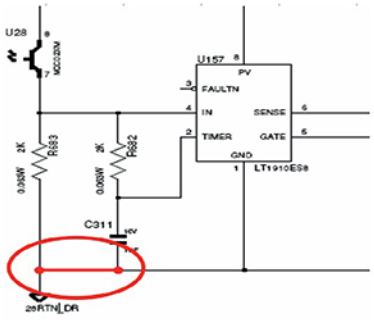
fiXtress ASR - Error Auto-Spotter

fiXtress Automated Schematic Review (ASR) is a Rule Based Logical and Parametric Schematic Verification tool which automatically detects hidden design errors using BQR's proprietary advanced algorithms.
fiXtress ASR uses the design BOM, Netlist and Interconnection signals as inputs. Parts library models and parameters are uploaded and logical data such as net or pin names are parsed, in order to obtain useful information relating to the design.
fiXtress ASR includes predefined good engineering practice "Common Rules", and two sophisticated rules ("Chip Interconnection" and "PIN Type Mismatch"). The user can also add "User Defined Rules".
fiXtress ASR generates an error report categorized by severity, serving electronics engineers for prioritizing design error corrections.

ASR - Common Rules

#	Rule	In Use
1	Floating Pin	☑
2	Floating IC GND	☑
3	Output to Output	☑
4	Input to Input	☑
5	Output&Input Conflict	☑
6	Many Inputs to one Output	☑
7	Shorted 2-pin components	☑
8	RefDes missing in BOM	☑
9	Net with one connection	☑
10	Wrong IC Bus Connection	☑
11	Decoupling Capacitors	☑
12	No Signal for Input Pins	☑





ASR - Chip Interconnection Rules

Chip manufacturers provide Reference Designs for their chips, and their customers verify the compliance of their implementation with these recommendations. fiXtress ASR Chip Interconnection module performs this compliance check automatically. The module is a special Common Rule Test that checks the interconnection of two ICs according to a sequence of rules. The connection check is performed between groups of pins, such as the interconnection of an ASIC to a DDR memory chip.

ASR - PIN Type Mismatch Rules

The Pin Type Mismatch verification module detects a mismatch between the IC pin type assignment in the Schematics and the fiXtress Pin Library type assignment. This way, the component packaging mismatches are detected when the Schematics pin type is different than the one in the fiXtress pin Library (e.g. a certain IC pin is defined as an Output in the Schematics and as a Power pin in the fiXtress pin Library).

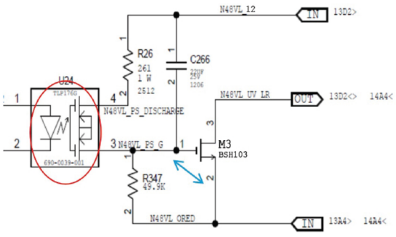
ASR - User Defined Rules

User Defined Rules (Project Rules or Connectivity Verification) are specific technology connectivity rules used for detecting connectivity issues such as Net name and power conflicts, ground and power supply issues, pull-up resistors on open drain outputs, etc. The rules defining objects that need to be connected/not-connected and the connecting elements are customizable, using a standard Regular Expression description.
BQR has developed pre-defined rules for various technologies such as: Open Drain/ Open Collector Pins, I2C, Crystal, NC pins, PCIe differential, PECL Terminations, Clock AC/TAC and more.
fiXtress ASR can be configured with an additional set of rules for Sneak Circuit Analysis.

fiXtress™
Variety of Modules

fiXtress Rapid

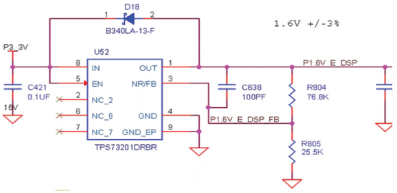
fiXtress Rapid performs automated Stress Calculation for incomplete designs in the Schematics Phase, using logical calculations, enabling multiple engineers to work concurrently on a single design. This analysis helps select the appropriate component rating before the final BOM freeze.
The schematic design represented by the BOM and Netlist is used to calculate the electrical stress of the components. The ground signals specification and ICD (Interface Control Document) data are also needed to set power input constraints. These calculations use data from the Components Database, which includes the components' electrical properties from the datasheet. The data is used to calculate DC operational parameters, such as power dissipation, voltage and current. Results are then provided to the Stress Derating Analysis module.



Sample detected error

fiXtress Precise

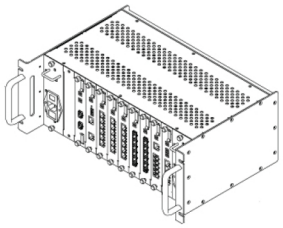
fiXtress Precise performs automated Stress Analysis for complete designs in the verification (pre-layout) phase, using a physical simulation. Accurate stress calculations are performed after the BOM freeze, providing actual operational parameters for all components in the circuit, such as power dissipation, voltage and current for a mixed signal, Analog, Digital, and RF including DC/DC power supplies. fiXtress Precise uses State Vectors for analog circuits, and Bus-Simulation for digital circuits. The results serve as guidance for smart component placement based on component power dissipation.



Sample detected error

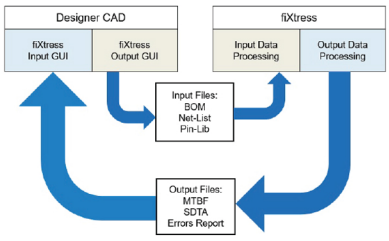
Multi-Boards Integration

Each PCB, when simulated and tested individually, can operate flawlessly, but when it is integrated with other boards, connection errors may arise, which can burn the PCB or generate malfunction on the system level. This module reduces such risks by verifying the connectivity between several PCBs and saves time otherwise wasted on redesign.



CAD/CAE/PLM Interfaces

fiXtress provides interfaces to a variety of tools, such as OrCAD, Cadence, Altium, Mentor, Agile-PLM, Intel and Excel, enabling retrieval of design data and libraries from these tools to the fiXtress simulator and component library database. fiXtress unique advantages include automated creation of a parts library by reusing the existing libraries' data in the CAD/CAE/PLM.



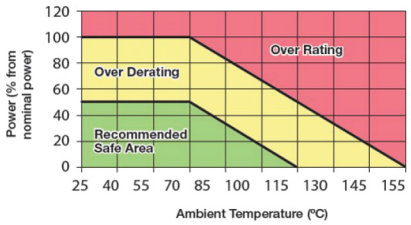
Mini Thermal Calculator

fiXtress uses the components package information and the calculated components' power dissipation to estimate the board's average temperature rise relative to the ambient temperature, as well as the individual junction temperature for active components.
The impact of different cooling methods (heat-sink, a selected airflow or a combination of methods) on various components or on the entire board can also be explored using fiXtress.

RefDes	Part Nu...	dT[°C]	T[°C]	Main Stress/C..	P-stress	V-stress	I-stress
System	PRSMT		50.0				
A1	DATA	24.5	74.5				
U31	AD573	7.0	81.5	Tj=116.3°C	0.316	15	---
Q21	20FQ04...	4.0	78.5	Tj=113.5°C	1	15	6
U22	LM117	0.0	74.5	Tj=109.5°C	0.5	15	0.5
Q11	2N6796	3.0	77.5	Tj=102.5°C	1	20	3
D31Z	1N4678	0.0	74.5	Tj=97.0°C	0.09	-	-
U21	MC6809E	0.0	74.5	Tj=88.5°C	0.2	5	0.005
U1	4192-08	0.0	74.5	Tj=83.4°C	-	-	-

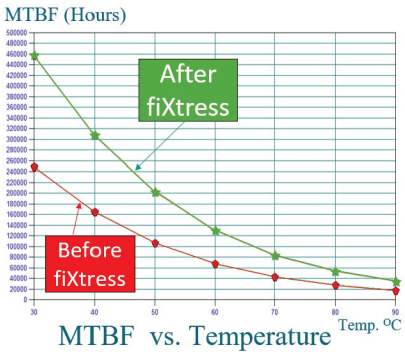
Stress Derating Analysis

Stress Derating Analysis helps designers select the appropriate components Rating according to stress load and temperature. Stress Derating Analysis compares the calculated worst-case electrical stress parameters (current, voltage, power, junction temperature etc.) with the maximum component rating and predefined derating profile, to detect over-Rating (red) and over-derated (yellow) components. The derating profile can be customized by users according to their own practices. Over-designed components are also detected when stress is much lower than rating. The software generates thermal placement guidelines in the form of a Pareto list, for optimal placement during layout.



MTBF

The Mean Time Between Failure (MTBF) module predicts component failure rates and presents the MTBF result for each component and assembly in a system tree using a serial reliability model. Component failure rates are predicted according to the following models: Mil-HDBK-217-F2/G, Telcordia-3, IEC-62308, SN-29500 Siemens, FIDES, GJB299, HRD-4 and Rel-Tools -non-operation, including customized user defined models. Calculations can combine multiple prediction methods in a single project.



Testimonials

"fiXtress helps us accelerate our efforts to perform automated design reviews, electrical stress analysis and reliability prediction prior to PCB layout and manufacturing. It is both a time-saver and a productivity enhancer."
Dr. Josh Liew, Reliability Program Manager, Baker Hughes

"BQR's team performed electrical stress analysis for our company using fiXtress. FiXtress reports, which detected several design errors, helped us improve PCB reliability and robustness and saved us considerable time and expenditures".
David Asher, Team Leader, Elbit systems

"With fiXtress ASR, we went from entire days of manual checks to an effective automated process lasting just several moments. Best of all, now we can be sure that the chip is used correctly by every single car manufacturer".
Israel Bar, Hardware Design Engineer, Mobileye

BQR Company Profile

BQR is a world leader in reliability analysis and maintenance optimization solutions for the EDA market. BQR software tools help engineers create more robust and reliable products, as well as improving the design process.

Throughout its 25 years of experience, the company serves leading companies in Israel and worldwide, including Elbit, IAI, DSO, Israel Electric Corporation, Cisco, Baker-Hughes, IBM, Philips, Bombardier, Schiphol Airport, Mobileye and others.

BQR Reliable Engineering Optimized Maintenance
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